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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,521	06/19/2003	Nguyen Xuan Nguyen	B-3863NP 620845-2	8663

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,521	NGUYEN ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover she t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-32 is/are pending in the application.

4a) Of the above claim(s) 17-32 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 June 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 20040322.+20030902
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1 – 16 in Paper No. 20040415 is acknowledged. The traversal is on the ground(s) that "In view of the expense that would be imposed upon the Applicant by multiple patent applications and multiple patents, it is believed that restriction requirements should be issued only when absolutely necessary." This is not found persuasive because a proper restriction requirement was given in the paper dated March 17, 2004 and applicant's response does not point out any supposed errors in the restriction requirement.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 17 – 32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected group, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 20040415.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 6, 9 – 11, and 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama et al. (USPAT 6492669, Nakayama) in view of the applicant's admitted prior art (AAPA).

With regard to claim 1, Nakayama discloses in figure10 a process for fabricating ohmic contacts (8 and 9) in a field-effect transistor. Nakayama discloses in figure 10 the transistor comprising a layered semiconductor structure. Nakayama discloses in figure 10 the transistor comprises a group III nitride compound first semiconductor layer (6) having a first band gap. Nakayama teaches in column 8, lines 22 – 26 that each layer of the transistor may be doped with a charge carrier. It is not clear in Nakayama if the first semiconductor layer is specifically doped with a charge carrier. AAPA teaches in figure 1 and paragraph [0006] a first semiconductor layer (9) doped with a charge carrier. It would have been obvious to one of ordinary skill in the art at the time of the present invention to have the doped charge carrier of the AAPA in the first semiconductor layer of Nakayama in order to dope each layer of the stack of semiconductor layers appropriately as stated by Nakayama in column 8, lines 22 – 26. Nakayama discloses in figure 10 a group III nitride compound second semiconductor layer (3) having a second band gap that is less than the first band gap and positioned below the first semiconductor layer to generate an electron gas in the semiconductor structure. It should be noted that the claim limitation "to generate an electron gas in the semiconductor structure" is an intended use and/or functional language recitation that does not bear any patentable weight in this method claim, however, it is met by the combination of Nakayama and the AAPA. Nakayama discloses in figure 10, column 9, lines 1 – 34, and column 10, line 63 – column 11, line 8 thinning the first semiconductor layer, forming recessed portions in the first semiconductor layer. Nakayama discloses in figure 10 and

column 9, lines 20 – 27 depositing ohmic contacts (8 and 9) over the recessed portions, and heating (annealing) the deposited ohmic contacts, whereby, after the heating step, the ohmic contacts communicate with the electron gas. It should be noted that the claim limitation "the ohmic contacts communicate with the electron gas" is an intended use and/or functional language recitation that does not bear any patentable weight in this method claim, however, it is met by the combination of Nakayama and the AAPA.

With regard to claim 2, Nakayama discloses in figure 10 and column 8, lines 49 – 54 wherein the first semiconductor layer comprises aluminum gallium nitride (AlGaN, when $x<1$ and $y>0$) and the second semiconductor layer comprises gallium nitride (GaN).

With regard to claim 3, Nakayama discloses in figure 10, column 9, lines 20 – 27 and column 10, lines 15 – 23 the ohmic contacts comprise titanium, aluminum, and gold. Nakayama further discloses in column 10, lines 15 – 23 wherein the ohmic contacts may comprise a metal which forms an ohmic contact with the second semiconductor layer. Nakayama is silent to the ohmic contacts specifically comprising titanium, aluminum, nickel and gold. The AAPA further teaches in paragraph [0005] ohmic contacts that comprise titanium, aluminum, nickel and gold. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ohmic contacts of the AAPA in the method of Nakayama in order to use a metal layer creating ohmic contact that penetrates to the second semiconductor layer as taught by Nakayama in column 10, lines 15 – 23 and the AAPA in paragraph [0005].

With regard to claim 4, the AAPA further teaches in paragraph [0005] wherein the ohmic contacts comprise 6% titanium, 65% aluminum, 13% nickel, and 16% gold.

With regard to claim 5, Nakayama discloses in column 9, lines 20 – 27 and column 10, line 63 – column 11, line 8 wherein the step of thinning the first semiconductor layer is performed through a reactive ion etching (RIE) process (electron cyclotron resonance plasma reactive ion etching (ECR) is a type of reactive ion etching (RIE)).

With regard to claim 6, Nakayama discloses in column 9, lines 20 – 27 and column 10, line 63 – column 11, line 8 wherein the reactive ion etching (RIE) process employs chlorine (Cl_2).

With regard to claim 9, Nakayama discloses in figure 10 wherein the ohmic contacts are source ohmic contacts (8).

With regard to claim 10, Nakayama discloses in figure 10 wherein the ohmic contacts are drain ohmic contacts (9).

With regard to claim 11, AAPA further teaches in paragraph [0005] wherein the ohmic contacts are heated at a temperature of about 875 °C ("e.g., 900 °C" as taught in paragraph [0005] is about 875 °C).

With regard to claim 14, similar to claim 3 above, the AAPA teaches in paragraph [0005] wherein the ohmic contacts are made of a metal system comprising a plurality of metals, and wherein the step of heating alloys the ohmic contacts.

With regard to claim 15, the AAPA teaches in paragraph [0005] wherein the metal system comprises titanium, aluminum, nickel and gold.

With regard to claim 16, Nakayama discloses in figure 10, and column 5, lines 25 – 55 wherein the field-effect transistor is a heterojunction field-effect transistor (HJFET).

5. Claims 7, 8, 12, and 13are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama and the AAPA as applied to claims 1, 5, and 6, respectively, above, and further in view of one of ordinary skill in the art.

With regard to claim 7, Nakayama discloses in figure 10, column 9, lines 20 – 27 and column 10, line 63 – column 11, line 8 wherein the reactive ion etching process (RIE) thins the first semiconductor layer. It is not clear if the reactive ion etching process (RIE) of Nakayama thins the first semiconductor layer according to a linear function of time. Etch rate is a parameter of a normal etch process that one of ordinary skill in the art would recognize as a linear function of time, and therefore, one of ordinary skill in the art would recognize that a the reactive ion etching process (RIE) that thins the first semiconductor layer according to a linear function of time would be desirable. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use an etch rate which thins the first semiconductor layer according to a linear function of time in the process of Nakayama and the AAPA in order to control the thinning process over a known time period so that all of the first semiconductor layer is not etched away.

With regard to claim 8, one of ordinary skill in the art would recognize that Nakayama discloses in figure 10 wherein RIE process has an etching time. Nakayama and the AAPA are silent to an etch rate for the first semiconductor layer. One of ordinary skill in the art would further recognize that the etch rate of the method may be optimized in such a way as to choose an etch rate wherein the RIE process has an etching time of about 45 seconds (see MPEP 2144.05).

With regard to claim 12, Nakayama discloses in figure 10 wherein the recessed portions in the first semiconductor layer have a thickness corresponding to about 2/3 of the thickness of the first semiconductor layer. Nakayama and the AAPA are silent to wherein the recessed portions in the first semiconductor layer have a thickness corresponding to 2/3 of the thickness of the first semiconductor layer. One of ordinary skill in the art would recognize that the recessed portions in the first semiconductor layer could have a thickness corresponding to 2/3 of the thickness of the first semiconductor layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to have 2/3 of the thickness of the first semiconductor layer thinned in Nakayama in order to optimize the performance of the device by optimizing the thickness of the first semiconductor layer under the ohmic contacts. (See MPEP 2144.05).

With regard to claim 13, Nakayama discloses in column 9, lines 1 – 14 wherein the thickness of the first semiconductor layer is about 100 angstroms. Nakayama is silent to a first semiconductor thickness of 300 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a first semiconductor layer with at thickness of 300 angstroms in the method of Nakayama and the AAPA there is no evidence indicating that a thickness of 100 angstroms is critical, and this thickness may be optimized for the given process and device. (See MPEP 2144.05). Therefore, according to claim 12, the thickness of the recessed portions is about 200 Angstrom.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ando et al. and Ishikawa et al. both disclose recessing a first semiconductor layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II